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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. Sakata et al

Serial No. 10/600,541 Group Art Unit: 2133

Filed: June 23, 2003 Examiner: J. Torres

For: SEMICONDUCTOR INTEGRATED CIRCUIT WITH MEMORY REDUNDANCY CIRCUIT

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22314-1450

Sir:

In response to the Office Action dated June 16, 2004, Applicants elect Group 1, claims 1-7 without traverse.

Please charge any additional fees resulting from this action to Deposit Account No. 50-1417.

Respectfully submitted,

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